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EXAMINER	
VO, TED T	

ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/998,848	OGAMI, KENNETH Y.	
	Examiner	Art Unit	
	Ted T. Vo	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 16-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 16-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed on 03/14/2005 responsive to the Office action dated, 12/21/04.

Within the amendment: Claims 1, 11, 13-14, 16-26, 29, and 31-32 are amended. Claim 15 is canceled.

Within this detailed action,

New ground of rejection to Claims 1-14, 16-35 is presented in this Office action. Because the amendment necessitated the new ground(s) of rejection, accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Claims 1-14, 16-35 are pending in this application.

Response to Arguments

2. Applicants' arguments in the Remarks section filed on 03/14/2005 have been fully considered.

All Applicants' arguments, which are related to the newly amended limitations, are moot in view of the new ground of rejection.

However, to clarify the position of the rejection and the use of the prior arts, following Applicants remarks filed on 03/14/2005 will be respectfully responded: For example:

With regards to Applicants' recognition that Tutor, Tech, Forum, and IDE references do not qualify as prior art under 35 USC 102(b) (Remarks: page 13, third paragraph). Examiner respectfully responds that under this new ground of rejection, Bindra, the anticipated reference, addressed the PSoC Designer known more than a year before the effective filing date of this application. Other references Tutor, Tech, Forum (still qualifying prior arts) disclosed/mentioned the "PSoC Designer" which has been known for more than a year before the filing of this application. The IDE reference is withdrawn as being unqualified prior art.

With regards to Applicants' address of the Tutor where Applicants point to page 15 and 16 of this reference and the arguments that the user manually enters source code that does not teach automatically generating source code (Remarks: page 14, first full paragraph), and the argument that Office Action do not show or suggest "automatically constructing source code/assembly code" (Remarks: pages 14-16).

Examiner respectfully responds that tool "PSoC Designer" shown by Figure 4 of Bindra and the tool PSoC Designer of the Tutor are the **same tool**. The Tutor aims to teach/**to tutor** a user how to update, to modify "User module"; i.e., the user could make or update a "use module" which is typically shown under icons. Each user module is functionalized as a circuit element in a real circuit design. Actually, the code in each of "user modules" will be automatically received by the TOOL, "PSoC Designer". This tool will construct the whole code (source code/assembly code) in accordance to the input information, where the whole code represents a real circuit design in which each user module is a circuit element. The Tutor has addressed the PSoC Designer" that automatically does the generation of the whole code,

> "When you generate "application files", PSoC Designer takes all Device Configurations and updates existing assembly-source code and C compiler code files (including the project library source, PSoConfig.asm) and generate API (Application Program interface) and ISR (Interrupt Service Routine) Shells"(Tutor: page 14).

It should be noted that the Tutor only tutors a user. The PSoC Designer comprising the features pointed out by Examiner above (Tutor: page 14) automatically constructs the code in the manner of the Claims, "*Receiving a selection of a user module*" and "*automatically constructing source code comprising configuring information*" as recited in such manners in Claims 1, 13, 17, 21, 25, 26, and 31.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 1-14, 16-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bindra, "Programmable SoC Delivers A New Level Of System Flexibility", 2000, in view of Tutorial Revision 1.0 (hereinafter: Tutor), "PSoC Designer: Integrated Development Environment", 7-2001.

Given the broadest reasonable interpretation of followed claims in light of the specification.

As per Claim 1:

Bindra discloses a PSoC Designer that is used to configure and construct code for a microcontroller; the disclosure covers the limitations,

A method for configuring a microcontroller, comprising:

displaying a collection of virtual blocks in a design system with each virtual block in said collection corresponding to a programmable block in said microcontroller (Bindra: See P.11, Figure 4);

receiving a selection of a user module defining a function (Bindra: See Figure 4: "User Modules Selected for Placement": E.g. see circuit block icons in the right top section which will be implemented in a combination shown within the right bottom section in the Figure 4);

assigning a virtual block taken from said collection to said user module (See Figure 4, Each block in the circuit in the right bottom section in Figure 4 could be assigned in this section from selection of

"User Modules" in the right top section; configuration information and connection are assigned by dialog section in the left section and the buttons given in the top rows of the PSoC Designer Tool); *automatically constructing source code comprising configuration information for a programmable block of said microcontroller corresponding to said virtual block wherein said configuration information is used to cause said programmable block to implement said function* (Bindra: For this limitation, see Figure 4 and its below illustration: "which are next mapped onto the SoCblocks on-chip". For *configuration information*: refer to "Global Resources" and "Placement parameters" in the left section of Figure 4).

Bindra does not explicitly address the "PSoC Designer" to do the "*automatically constructing source code*".

The Tutor, "PSoC Designer: Integrated Development Environment" teaches "*automatically constructing source code comprising configuration information*" (Tutor: See whole page 14) for the circuit in Figure 4 of Bindra. Particularly, in Tutor, page 14, see text pointed by the symbol '=>' and see Figure 13, and refer "The Application code has been generated successfully'. For *configuration information*: refer to Figures 7-9 in pages 10-11.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include, the teaching "*automatically constructing source code comprising configuration information*" of Tutor to the disclosure of Bindra. The motivation would be obvious because the Tool used in the Tutor and the Tool disclosed by Bindra are the same, and thus would provide self-learning to a designer and the designer thus lets the tool to automatically generate the combined functions implemented for his/her designs.

As per Claim 2: Bindra further discloses,

The method of Claim 1, wherein said function comprises a pulse width modulator (Bendra: See Figure 4, refer to "User Module" that represents various Digital functions, and see P.2 line 36, "PWMs").

As per Claim 3: Bindra further discloses, *The method of Claim 1, wherein said function comprises a timer.* (Bendra: See Figure 4, refer to "User Module" that represents various Digital functions, and see P.2 line 36, "*timers*").

As per Claim 4: Bindra further discloses, *The method of Claim 1, wherein said function comprises an analog-to-digital converter* (Bendra: See Figure 4, refer to "User Module" that represents various Digital functions, and see P.2 line 35, "ADCs").

As per Claim 5: Bindra further discloses, *The method of Claim 1, wherein said function comprises a digital-to-analog converter* (Bendra: See Figure 4, refer to "User Module" that represents various Digital functions, and see P.2 line 35 "DACs").

As per Claim 6: Bindra further discloses, *The method of Claim 1, wherein said function comprises a counter* (Bendra: See Figure 4, refer to "User Module" that represents various Digital functions, and see P.2 line 36 "counters").

As per Claim 7: Bindra further discloses, *The method of Claim 1, wherein said function comprises a signal amplifier.* (See Figure 4, refer to "User Module" that represents various Digital functions, and see P.2 line 33 *"differential amplifiers"*).

As per Claim 8: Bindra further discloses, *The method of Claim 1, wherein said function provides serial communication.* (See Figure 4, refer to "User Module" that represents various Digital functions, and see P.3, line 9, "serial transmitters/receivers").

As per Claim 9: Bindra further discloses, *The method of Claim 1, wherein said collection is displayed as a two dimensional array of programmable analog virtual blocks and programmable digital virtual blocks.* (See collections in the right bottom section, which is *two dimensional array*).

As per Claim 10: Bindra further discloses, *The method of Claim 1, wherein said assigning further comprises assigning a second virtual block to said user module* (See collections in the right bottom section, which is two *dimensional array*).

As per Claim 11: Bindra further discloses, *The method of Claim 1, wherein said source code comprises a symbolic name for a register address in said programmable block.* (Bendra: See page 2, lines 12-17 ('register space that holds the configuration information').

As per Claim 12: Bindra further discloses, *The method of Claim 11 wherein said symbolic name is derived from said function.* (See Bendra 'User module" in Figure 4, where user module represents a circuit element. Each circuit element is a symbolic name function: e.g.: ADC, DAC, Timer, Counter, etc).

As per Claim 13: Bindra disclosure covers the limitations,

A method of configuring a microcontroller having a programmable block, said method comprising:

receiving a selection of a user module defining a circuit design (Bindra: See Figure 4: "User Modules Selected for Placement": E.g. see circuit block icons in the right top section which will be implemented in a combination shown within the right bottom section in the Figure 4);

assigning a virtual block in a design system where said virtual block corresponds to said programmable block (See Figure 4, Each block in the circuit in the right bottom section in Figure 4 could be assigned in this section from selection of "User Modules" in the right top section; configuration information and connection are assigned by dialog section in the left section and the buttons given in the top rows of the PSoC Designer Tool); *and*

automatically constructing assembly code comprising configuration information for said programmable block to implement said circuit design, wherein said assembly code is constructed from template assembly code by substituting information specific to said user module and information specific to said circuit design for generic information in said template assembly code (Bindra: For this limitation, see Figure 4 and its illustration below the Figure, "which are next mapped onto the SoCblocks on-chip". For *configuration information*: refer to "Global Resources" and "Placement parameters" in the left section of Figure 4).

Bindra does not explicitly address the "PSoC Designer" to do the "*automatically constructing assembly code comprising configuration information".*

The Tutor, "PSoC Designer: Integrated Development Environment" teaches "*automatically constructing assembly code comprising configuration information"* (Tutor: See whole page 14; particularly see first full paragraph, "existing assembly-source": Claimed limitation: *from template assembly code*) for the circuit in Figure 4 of Bindra. Particularly, in Tutor, page 14, see text pointed by the symbol '=>' and see Figure 13, and refer "The Application code has been generated successfully'. For *configuration information*: refer to Figures 7-9 in pages 10-11 (Tutor).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include, the teaching "*automatically constructing assembly code comprising configuration information*" of Tutor to the disclosure of Bindra. The motivation would be obvious because the Tool used in the Tutor and the Tool disclosed by Bindra are the same, and thus would provide self-learning to a designer and the designer thus lets the tool to automatically generate the combined functions implemented for his/her designs.

As per Claim 14: Bindra in view of Tutor further discloses,

"The method of Claim 13, wherein said automatically constructing further comprises: computing a register address for a register within said programmable block; determining a symbolic name for said register address, said symbolic name corresponding to said user module and said circuit design; and substituting said symbolic name for a generic name in said template assembly code". See page 2, lines 12-17 ('register space that holds the configuration information') and page 6, lines 7- 13, ('user modules are selected, pins are assigned, and register mapping are establish') (Further refer to Tutor page 14 for *automatically constructing*) for cover the limitations:

- *computing a register address for a register within said programmable block:* referring "register mapping"
- *determining a symbolic name for said register address, said symbolic name corresponding to said user module and said circuit design:* referring "holds the configuration information".
- *substituting said symbolic name for a generic name in said template assembly code:* referring the code construction performed by the PSoC Designer shown by the Tutor.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine because the Tool, PSoC Designer, used in the Tutor and the Tool, PSoC Designer, disclosed by Bindra are the same.

As per Claim 16: Bindra in view of Tutor further discloses the limitations of Claim 16.

See page 2, lines 12-17 ('register space that holds the configuration information') and page 6, lines 7- 13, ('user modules are selected, pins are assigned, and register mapping are establish') (Further refer to Tutor page 14 for *automatically constructing*).

- determining a symbolic name corresponding to said user module and said circuit design; referring "holds the configuration information".

- computing a register address for a register within said programmable block; referring "register mapping"

- assigning said symbolic name to said register address; and placing said symbolic name into said assembly code in place of a generic name provided in said template assembly code file: referring the code construction performed by the PSoC Designer.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine because the Tool PSoC Designer used in the Tutor and the Tool PSoC Designer disclosed by Bindra are the same.

As per Claim 17: Bindra disclosure covers the limitations,

A method of configuring a microcontroller having a programmable block, said method comprising:

receiving a selection of a user module defining a function; (Bindra: See Figure 4: "User Modules Selected for Placement": E.g. see circuit block icons in the right top section which will be implemented in a combination shown within the right bottom section in the Figure 4);

assigning a virtual block in a design system where said virtual block corresponds to said programmable block (See Figure 4, Each block in the circuit in the right bottom section in Figure 4 could be assigned in this section from selection of "User Modules" in the right top section; configuration information and connection are assigned by dialog section in the left section and the buttons given in the top rows of the PSoC Designer Tool); *and*

automatically constructing assembly code with personalization information specifying said programmable block as performing said function, wherein said assembly code is constructed from template assembly code by substituting information specific to said user module and information specific to said function for generic information in said template assembly code (Bindra: For this limitation, see Figure 4 with its illustration below, "which are next mapped onto the SoCblocks on-chip". For *personalization information*: refer to "Global Resources" and "Placement parameters" in the left section of Figure 4).

Bindra does not explicitly address the "PSoC Designer" to do the "*automatically constructing assembly code with personalization information specifying said programmable block as performing said function*".

The Tutor, "PSoC Designer: Integrated Development Environment" teaches "*automatically constructing assembly code with personalization information specifying said programmable block as performing said function*" (Tutor: See whole page 14; particularly see first full paragraph, "existing assembly-source": Claimed limitation: *from template assembly code*) for the circuit in Figure 4 of Bindra. Particularly, in Tutor, page 14, see text pointed by the symbol '=>' and see Figure 13, and refer "The Application code has been generated successfully'. For *personalization information*: refer to Figures 7-9 in pages 10-11 (Tutor).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include, the teaching "*automatically constructing assembly code with personalization information*" of Tutor to the disclosure of Bindra. The motivation would be obvious because the Tool used in the Tutor and the Tool disclosed by Bindra are the same, and thus would provide self-learning to a designer and the designer thus lets the tool to automatically generate the combined functions implemented for his/her designs.

As per Claim 18: Bindra in view of Tutor further discloses,

"The method of Claim 17, wherein said automatically constructing further comprises:

computing a register address for a register within said programmable block;

determining a symbolic name for said register address, said symbolic name corresponding to said user module and said function; and

placing said symbolic name into said assembly code".

See page 2, lines 12-17 ('register space that holds the configuration information') and page 6, lines 7- 13, ('user modules are selected, pins are assigned, and register mapping are establish') (Further refer to Tutor page 14 for *automatically constructing*) for cover the limitations:

- *computing a register address for a register within said programmable block:* referring "register mapping"

- *determining a symbolic name for said register address, said symbolic name corresponding to said user module and said function:* refering "holds the configuration information".

- *placing said symbolic name into said assembly code:* refering the code construction performed by the PSoC Designer shown by the Tutor.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine because the Tool PSoC Designer used in the Tutor and the Tool PSoC Designer disclosed by Bindra are the same.

As per Claim 19: Regarding: *substituting said symbolic name in place of a generic name provided in said e template assembly code,* by refering the code construction performed by the PSoC Designer shown by the Tutor.

As per Claim 20: Bindra in view of Tutor further discloses the limitations of Claim 20.

See page 2, lines 12-17 ('register space that holds the configuration information') and page 6, lines 7- 13, ('user modules are selected, pins are assigned, and register mapping are establish') (Further refer to Tutor page 14 for *automatically constructing*).

- *determining a symbolic name corresponding to said user module and said function:* referring "holds the configuration information".

- *computing a register address for a register within said programmable block:* referring "register mapping".

assigning said symbolic name to said register address; and placing said symbolic name into said assembly code: refering the code construction performed by the PSoC Designer.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine because the Tool PSoC Designer used in the Tutor and the Tool PSoC Designer disclosed by Bindra are the same.

As per Claim 21: Regarding,

"*A method of configuring a microcontroller having a programmable block, said method comprising:*

receiving a selection of a user module defining a function having a control parameter;

assigning a virtual block in a design system where said virtual block corresponds to said programmable block; and

constructing assembly code for operating said control parameter within said programmable block, wherein said assembly code is constructed from template assembly code by substituting information specific to said user module, information specific to said function and information specific to said control parameter for generic information in said template assembly code".

Claim has the functionality corresponding to the functionality of Claim 17. See rationale addressed in the rejection of Claim 17 above.

As per Claim 22: Regarding, "*The method of Claim 21, wherein said constructing further comprises: computing a register address for a register within said programmable block; determining a symbolic name for said register address, said symbolic name corresponding to said user module and said function; and placing said symbolic name into said assembly code".*

Claim has the functionality corresponding to the functionality of Claim 18. See rationale addressed in the rejection of Claim 18 above.

As per Claim 23: Regarding, "*The method of Claim 22, wherein said placing further comprises: substituting said symbolic name in place of a generic name provided in said template assembly code".*

Claim has the functionality corresponding to the functionality of Claim 19. See rationale addressed in the rejection of Claim 19 above.

As per Claim 24: Regarding, "*The method of Claim 21, wherein said constructing further comprises: determining a symbolic name corresponding to said user module and said function; computing a register address for a register within said programmable block; assigning said symbolic name to said register address; and placing said symbolic name into said assembly code".*

Claim has the functionality corresponding to the functionality of Claim 20. See rationale addressed in the rejection of Claim 20 above.

As per Claim 25: Regarding,

"A method of configuring a microcontroller having a programmable block, said method comprising: receiving a selection of a user module defining a function having a control parameter;

assigning a virtual block in a design system where said virtual block corresponds to said programmable block;

constructing an assembly code routine using said control parameter, wherein said assembly code routine is constructed from template assembly code by substituting information specific to said user module, information specific to said function and information specific to said control parameter for generic information in said template assembly code; and constructing a header file referencing said assembly (Tutor: page 14: "project library source, PSoCConfig.asm" and/or "Application Program Interface", which are/is combined when generating Application files) *code routine".*

Claim has the functionality corresponding to the functionality of Claim 17. See rationale addressed in the rejection of Claim 17 above.

As per Claim 26:

Claim has the functionality corresponding to the functionality of Claim 1. See rationale addressed in the rejection of Claim 1 above.

As per Claim 27: Bendra further discloses, "two dimension array" (collection shown the right bottom section of Figure 4).

As per Claim 28: Bendra further discloses, "assigning a second virtual block" (which is either one of other blocks shown the right bottom section of Figure 4).

As per Claim 29: Bendra further discloses "assembly code" which is the code generated by the PSoC Design to the collection shown in the right bottom section of Figure 4, where the symbolic name for a register address is done by register mapping as addressed above.

As per Claim 30: Bendra further discloses, "derived from said function" which is based on the icon, "user module" which is functionalized to a circuit element, and based on pins assignment to the user module.

As per Claim 31: Bendra disclosure covers the limitation:

A computer implemented method of generating program information for a programmable electronic device, said method comprising:

a) accessing a selected a user module, wherein said user module is defined by a first data structure; (Bindra: See Figure 4: "User Modules Selected for Placement"- E.g. see circuit block icons in the right top section implemented in a combination shown within the right bottom section in the Figure 4);

b) placing said user module within a second data structure that defines a hardware resource of said programmable electronic device; (See Figure 4, Each block in the circuit in the right bottom section in Figure 4, could be assigned in this section from selection of " User Modules" in the right top section; configuration information and connection are assigned by dialog texts in the left section buttons on the top of the PSoC Designer Tool. When running the Tool, each user module assigned in the collection in the right bottom section will be assigned accordingly);

"c) using said first and second data structures to automatically generate first source code for realizing said user module within said hardware resource; and

d) saving said first source code in a computer file"

(Bindra: For this limitation, see Figure 4 and its below illustration: "which are next mapped onto the SoCblocks on-chip", '*using said first and second data structures*'. For *saving said first source code in a computer file*: refer to 'File", 'Edit', 'View' on the top of the PSoC Designer Tool).

Bindra does not explicitly address the "PSoC Designer" to do the "*automatically generate first source code for realizing said user module within said hardware resource*".

The Tutor, "PSoC Designer: Integrated Development Environment" teaches "*automatically generate first source code for realizing said user module within said hardware resource*" (Tutor: See whole page 14) for the circuit in Figure 4 of Bindra. Particularly, in Tutor, page 14, see text pointed by the symbol '=>' and see Figure 13, and refer "The Application code has been generated successfully'.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to include, the teaching "*automatically generate first source code for realizing said user module within said hardware resource*" in the Tutor to the disclosure of Bindra. The motivation would be obvious because the Tool used in the Tutor and the Tool disclosed by Bindra are the same, and thus would provide self-learning to a designer and the designer thus lets the tool to automatically generate the combined functions implemented for his/her designs.

As per Claim 32: Bindra in view of Tutor further discloses,

A method as described in Claim 31 further comprising:

e) accessing parameter values that define the behavior of said user module such that it operates in a prescribed manner; (Bindra: See left section in Figure 4);

f) automatically generating second source code, based on said parameter values, for causing said user module of said hardware resource to behave in said prescribed manner (See Tutor and its text discussed in page 14); *and*

g) saving said second source code in a computer file (Bendar: See Figure 4, icons in the top rows used to save a file).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine because the Tool PSoC Designer used in the Tutor and the Tool PSoC Designer disclosed by Bindra are the same.

As per Claim 33: Bendra further discloses, "*A method as described in Claim 32 further comprising using said first and second source code to program said programmable electronic device*" because it the collection in Figure 4 would be mapped to a real design.

As per Claim 34: Bendra further discloses, *A method as described in Claim 33 wherein said programmable electronic device is a microcontroller.* See Bendra's Figure 1.

As per Claim 35: Bendra in view of Tutor further discloses, *A method as described in Claim 31 wherein said a) and said e) are performed using a graphical user interface,* because PSoC Designer is a GUI.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of

this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (571) 272-3706. The examiner can normally be reached on 8:00AM to 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3694. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TUAN DAM
SUPERVISORY PATENT EXAMINER

Ted T. Vo
Patent Examiner
Art Unit 2192
June 10, 2005